

This listing of the claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

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1. (Amended) An apparatus for controlling a bank refresh including a plurality of banks, comprising:

a plurality of input buffer means for buffering bank address signals inputted from an external circuit with the command signal;

A, a counter for producing count signals, being reset by an output signals from the [N] plurality of input buffer means;

a switch means for combining the count signals from the counter in order to produce internal bank refresh signals in response to bank address signals from the [N] plurality of input buffer means; and

a chipset control means for generating a plurality of internal bank addresses for the refresh using the internal bank refresh signals,

wherein each input buffer means includes a latch means for sustaining the output signals of the plurality of input buffer means within a certain period of time only when the refresh command signals are applied.

2. (Amended) The apparatus as recited in claim 1, wherein ~~the number of the plurality of banks is  $2^N$~~ ; the number of the plurality of input buffer means is N, N is a positive integer, and the counter is (N-1)-nary, if the number of the plurality of banks is  $2^N$ .

3. Cancelled.

4. (Original) The apparatus as recited in claim 2, wherein the (N-1)-nary counter is reset by a logic combination of the bank address signals.

5. (Original) A method for controlling a bank refresh including  $2^N$  of banks, comprising the steps of:

- A<sub>1</sub>
- a) buffering N bank address signals inputted from the external circuit with the refresh command signals;
  - b) outputting the (N-1)-nary count signal in sequence by resetting at least one of N buffered signals;
  - c) switching and outputting unit of N-1 count signals to the bank refresh combination signals in response to the N buffered signals; and
  - d) generating an internal bank address for the refresh using the bank refresh combination signals.

6. (New) The apparatus as recited in claim 4, wherein N as an ~~positive integer~~ is at least three.

7. (New) The apparatus as recited in claim 5, wherein N is a positive integer and N is at least three.

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